

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115**General Description**

The AP2115 is CMOS process low dropout linear regulator with enable function, the regulator delivers a guaranteed 1A (min.) continuous load current.

The AP2115 features low power consumption.

The AP2115 is available in 1.2V, 1.8V, 2.5V and 3.3V regulator output, and available in excellent output accuracy $\pm 1.5\%$, it is also available in an excellent load regulation and line regulation performance.

The AP2115 is available in standard packages of SOIC-8 and SOT-89-5.

Features

- Output Voltage Accuracy: $\pm 1.5\%$
- Output Current: 1A (Min.)
- Fold-back Short Current Protection: 50mA
- Low Dropout Voltage (3.3V): 450mV (Typ.) @ $I_{OUT}=1A$
- Stable with 4.7 μ F Flexible Cap: Ceramic, Tantalum and Aluminum Electrolytic
- Excellent Line Regulation: 0.02%/V (Typ.), 0.1%/V (Max.) @ $I_{OUT}=30mA$
- Excellent Load Regulation: 0.2%/A @ $I_{OUT}=1mA$ to 1A
- Low Quiescent Current: 60 μ A (1.2V/1.8V/2.5V)
- Low Output Noise: 30 μ V_{RMS}
- PSRR: 68dB @ Freq=1kHz (1.2V/1.8V)
- OTSD Protection
- Operation Temperature Range: -40°C to 85°C
- ESD: MM 400V, HBM 4000V

Applications

- LCD Monitor
- LCD TV
- STB

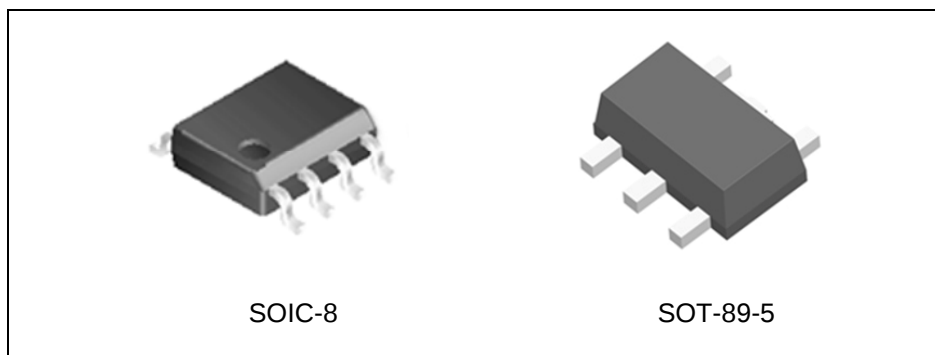
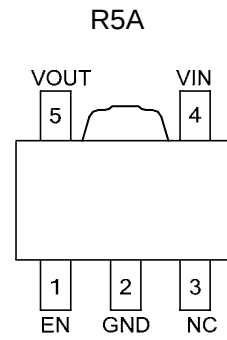
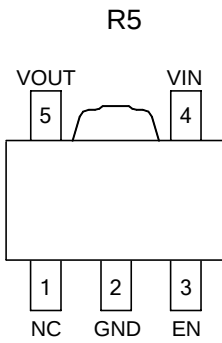


Figure 1. Package Types of AP2115

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115

Pin Configuration

R5 Package
(SOT-89-5)



M Package
(SOIC-8)

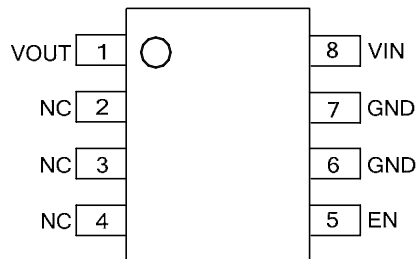


Figure 2. Pin Configuration of AP2115 (Top View)

Pin Descriptions

Pin No.		Name	Function
SOT-89-5	SOIC-8		
1	2, 3, 4	NC/EN	No connection/Chip Enable
2	6, 7	GND	GND
3	5	EN/NC	Chip Enable, H – normal work, L – shutdown output/ No Connection
4	8	VIN	Input Voltage
5	1	VOUT	Output Voltage

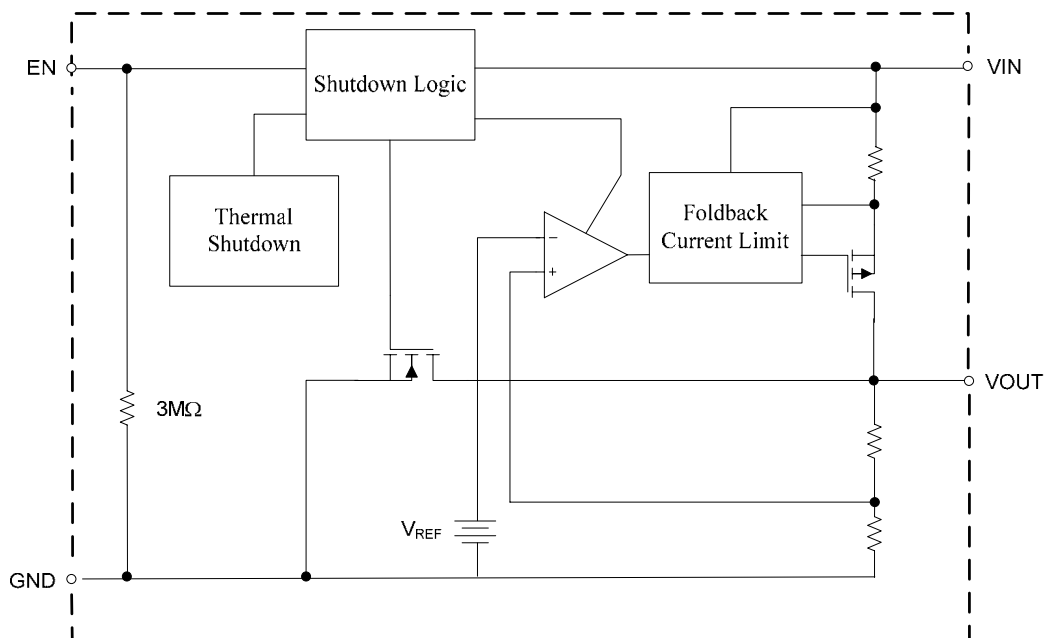
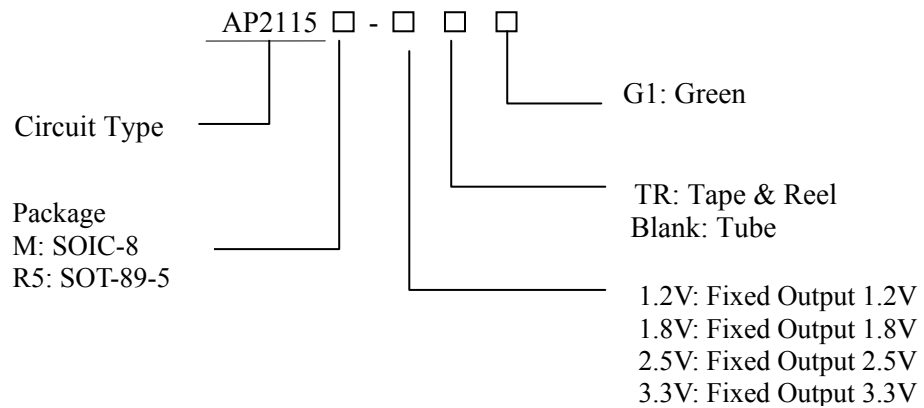
1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115**Functional Block Diagram**

Figure 3. Functional Block Diagram of AP2115

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Ordering Information**

Package	Temperature Range	Condition	Part Number	Marking ID	Packing Type
SOIC-8	-40 to 85°C	1.2V	AP2115M-1.2G1	2115M-1.2G1	Tube
			AP2115M-1.2TRG1	2115M-1.2G1	Tape & Reel
		1.8V	AP2115M-1.8G1	2115M-1.8G1	Tube
			AP2115M-1.8TRG1	2115M-1.8G1	Tape & Reel
		2.5V	AP2115M-2.5G1	2115M-2.5G1	Tube
			AP2115M-2.5TRG1	2115M-2.5G1	Tape & Reel
SOT-89-5	-40 to 85°C	3.3V	AP2115M-3.3G1	2115M-3.3G1	Tube
			AP2115M-3.3TRG1	2115M-3.3G1	Tape & Reel
		1.2V (R5)	AP2115R5-1.2TRG1	G22G	Tape & Reel
		1.8V (R5)	AP2115R5-1.8TRG1	G22H	Tape & Reel
SOT-89-5	-40 to 85°C	2.5V (R5)	AP2115R5-2.5TRG1	G37H	Tape & Reel
		3.3V (R5)	AP2115R5-3.3TRG1	G41H	Tape & Reel
		1.2V (R5A)	AP2115R5A-1.2TRG1	G27D	Tape & Reel
		1.8V (R5A)	AP2115R5A-1.8TRG1	G27G	Tape & Reel
SOT-89-5	-40 to 85°C	2.5V (R5A)	AP2115R5A-2.5TRG1	G41F	Tape & Reel
		3.3V (R5A)	AP2115R5A-3.3TRG1	G41G	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.5	V
Operating Junction Temperature Range	T_J	150	°C
Storage temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	°C
ESD (Machine Model)		400	V
ESD (Human Body Model)		4000	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{IN}	2.5	6.0	V
Ambient Operation Temperature Range	T_A	-40	85	°C

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Electrical Characteristics****AP2115-1.2 Electrical Characteristics (Note 2)**

$V_{IN}=2.5V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A=25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_J \leq 85^\circ C$ ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=2.5V$, $1mA \leq I_{OUT} \leq 30mA$	$V_{OUT} \times 98.5\%$	1.2	$V_{OUT} \times 101.5\%$	V
Input Voltage	V_{IN}				6	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=2.5V$, $V_{OUT}=1.182V$ to $1.218V$	1			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{IN}=2.5V$, $1mA \leq I_{OUT} \leq 1A$		0.2	1	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$2.5V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$	-0.1	0.02	0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1.0A$		1200	1300	mV
Quiescent Current	I_Q	$V_{IN}=2.5V$, $I_{OUT}=0mA$		60	75	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=2.5V$, $I_{OUT}=100mA$ $f=100Hz$		68		dB
		$f=1KHz$		68		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$, $T_A = -40^\circ C$ to $85^\circ C$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$ (No Load)		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	t_s	No Load		20		μs
EN Pull Down Resistor	R_{PD}			3.0		M Ω
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance	θ_{JC}	SOIC-8		74.6		$^\circ C/W$
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Electrical Characteristics (Continued)****AP2115-1.8 Electrical Characteristics (Note 2)**

$V_{IN}=2.8V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A=25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_J \leq 85^\circ C$ ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=2.8V$, $1mA \leq I_{OUT} \leq 30mA$	$98.5\% \times V_{OUT}$	1.8	$101.5\% \times V_{OUT}$	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=2.8V$, $V_{OUT}=1.773V$ to $1.827V$	1			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{IN}=2.8V$, $1mA \leq I_{OUT} \leq 1A$		0.2	1	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$2.8V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$	-0.1	0.02	0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1.0A$		500	750	mV
Quiescent Current	I_Q	$V_{IN}=2.8V$, $I_{OUT}=0mA$		60	75	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=2.8V$, $I_{OUT}=100mA$	$f=100Hz$	68		dB
			$f=1KHz$	68		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$, $T_A=-40^\circ C$ to $85^\circ C$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$ (No load)		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	t_S	No Load		20		μs
EN Pull Down Resistor	R_{PD}			3.0		$M\Omega$
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance	θ_{JC}	SOIC-8		74.6		$^\circ C/W$
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Electrical Characteristics (Continued)****AP2115-2.5 Electrical Characteristics (Note 2)**

$V_{IN}=3.5V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A=25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_J \leq 85^\circ C$ ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=3.5V$, $1mA \leq I_{OUT} \leq 30mA$	$98.5\% \times V_{OUT}$	2.5	$101.5\% \times V_{OUT}$	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=3.5V$, $V_{OUT}=2.463V$ to $2.537V$	1			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{OUT}=2.5V$, $V_{IN}=V_{OUT}+1V$ $1mA \leq I_{OUT} \leq 1A$		0.2	1	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$3.5V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$	-0.1	0.02	0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1A$		450	750	mV
Quiescent Current	I_Q	$V_{IN}=3.5V$, $I_{OUT}=0mA$		60	80	μA
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=3.5V$, $I_{OUT}=100mA$	$f=100Hz$	65		dB
			$f=1KHz$	65		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Start-up Time	t_S	No Load		20		μs
EN Pull Down Resistor	R_{PD}			3.0		$M\Omega$
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance	θ_{JC}	SOIC-8		74.6		$^\circ C/W$
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Electrical Characteristics (Continued)****AP2115-3.3 Electrical Characteristics (Note 2)**

$V_{IN}=4.3V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A=25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_J \leq 85^\circ C$ ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=4.3V$, $1mA \leq I_{OUT} \leq 30mA$	$98.5\% \times V_{OUT}$	3.3	$101.5\% \times V_{OUT}$	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=4.3V$, $V_{OUT}=3.25V$ to $3.35V$	1			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{IN}=4.3V$, $1mA \leq I_{OUT} \leq 1A$		0.2	1	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$4.3V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$	-0.1	0.02	0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1A$		450	750	mV
Quiescent Current	I_Q	$V_{IN}=4.3V$, $I_{OUT}=0mA$		65	90	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=4.3V$, $I_{OUT}=100mA$	$f=100Hz$	65		dB
			$f=1KHz$	65		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$ (No load)		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	t_S	No Load		20		μs
EN Pull Down Resistor	R_{PD}			3.0		$M\Omega$
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance	θ_{JC}	SOIC-8		74.6		$^\circ C/W$
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.

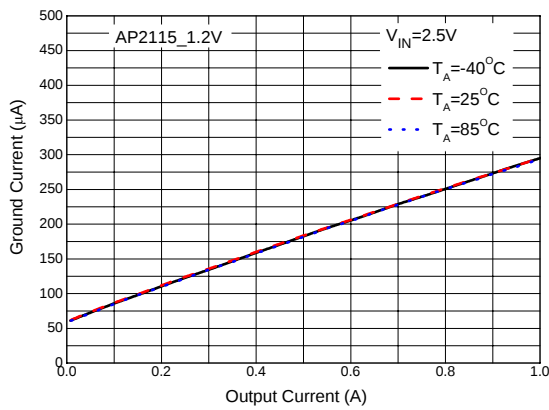
**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Typical Performance Characteristics**

Figure 4. Ground Current vs. Output Current

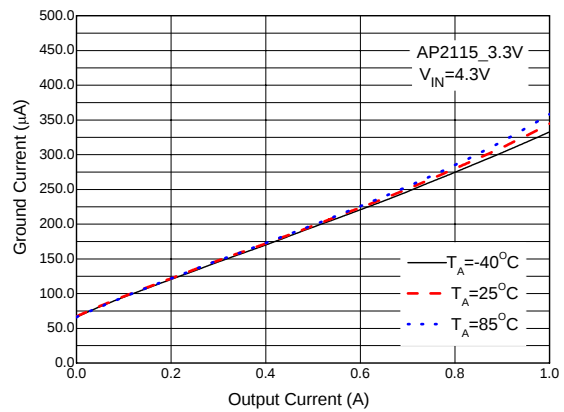


Figure 5. Ground Current vs. Output Current

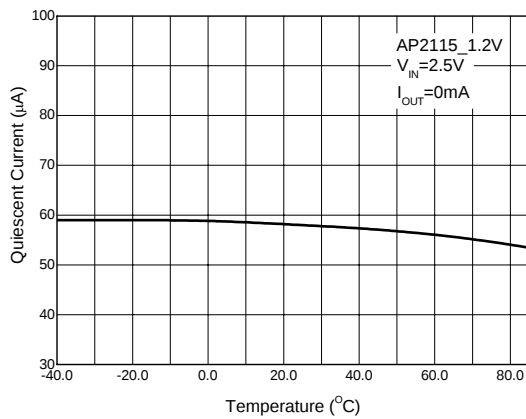


Figure 6. Quiescent Current vs. Temperature

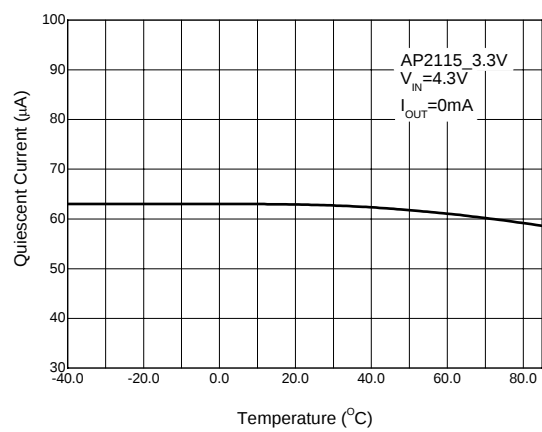


Figure 7. Quiescent Current vs. Temperature

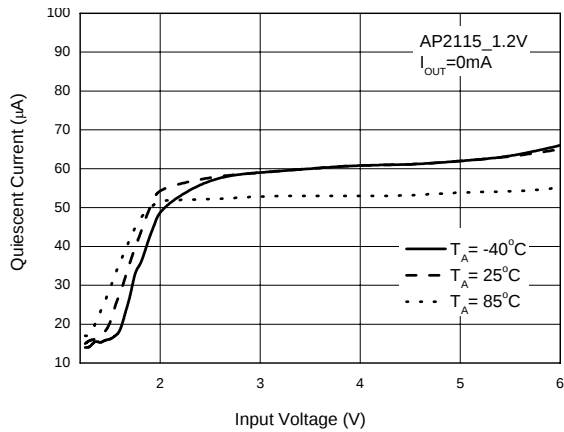
**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Typical Performance Characteristics (Continued)**

Figure 8. Quiescent Current vs. Input Voltage

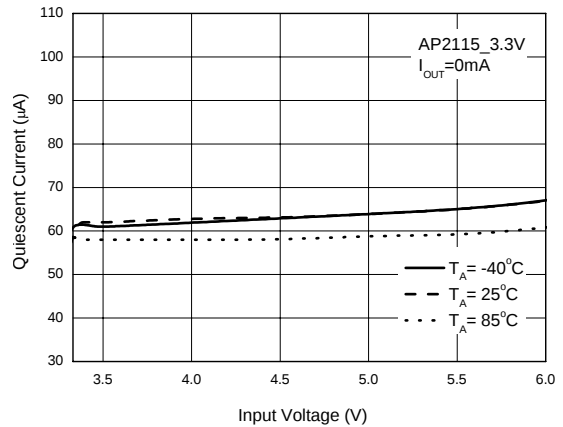


Figure 9. Quiescent Current vs. Input Voltage

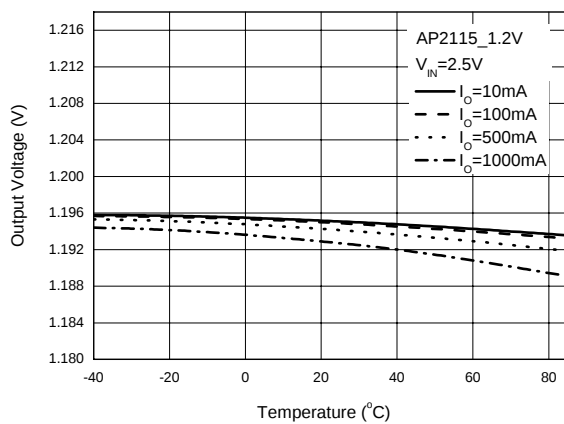


Figure 10. Output Voltage vs. Temperature

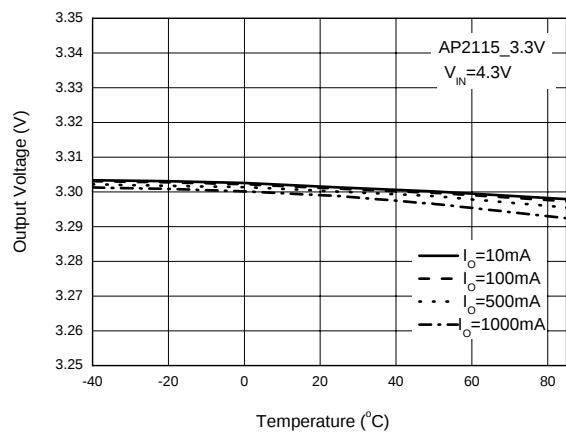


Figure 11. Output Voltage vs. Temperature

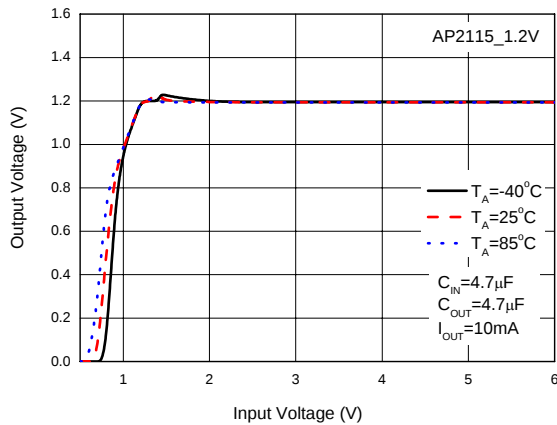
**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Typical Performance Characteristics (Continued)**

Figure 12. Output Voltage vs. Input Voltage

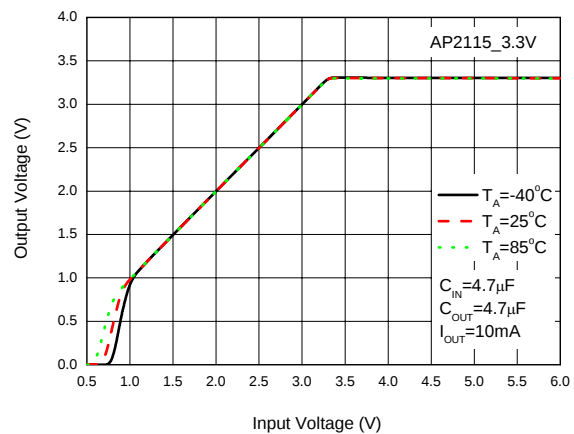


Figure 13. Output Voltage vs. Input Voltage

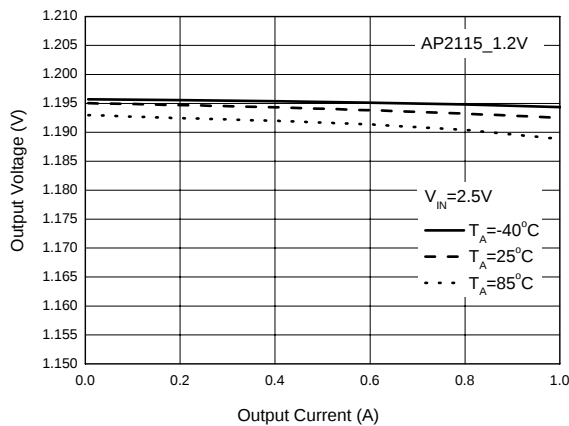


Figure 14. Output Voltage vs. Output Current

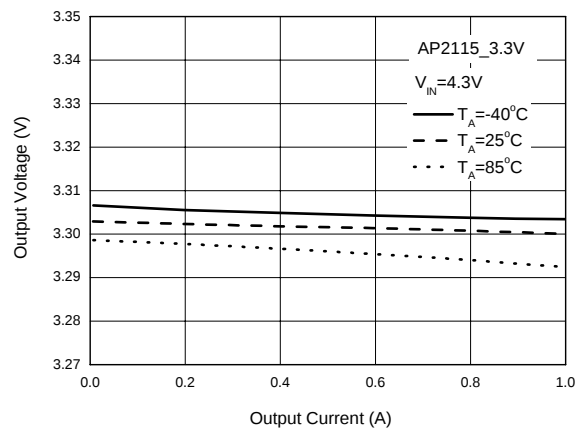


Figure 15. Output Voltage vs. Output Current

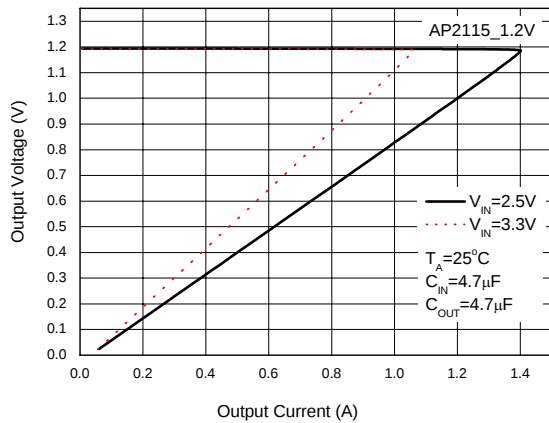
**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Typical Performance Characteristics (Continued)**

Figure 16. Output Voltage vs. Output Current

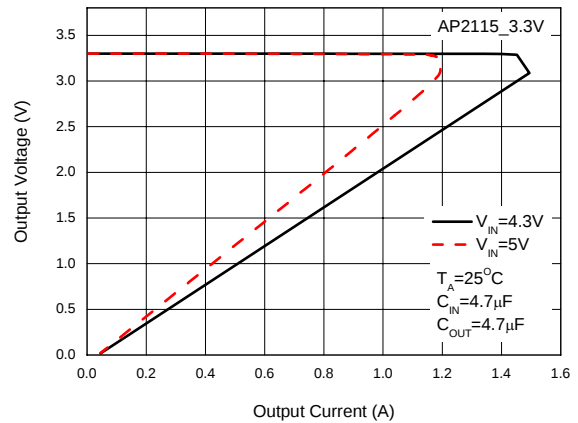


Figure 17. Output Voltage vs. Output Current

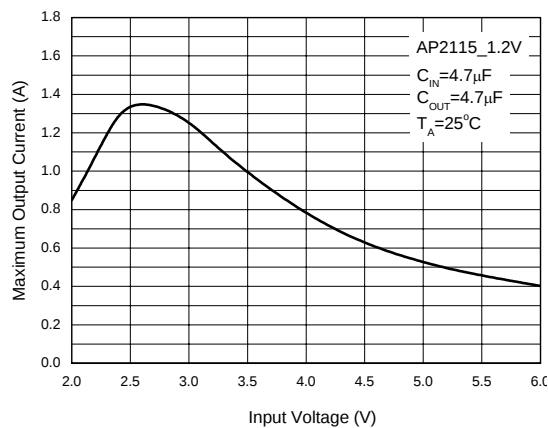


Figure 18. Maximum Output Current vs. Input Voltage

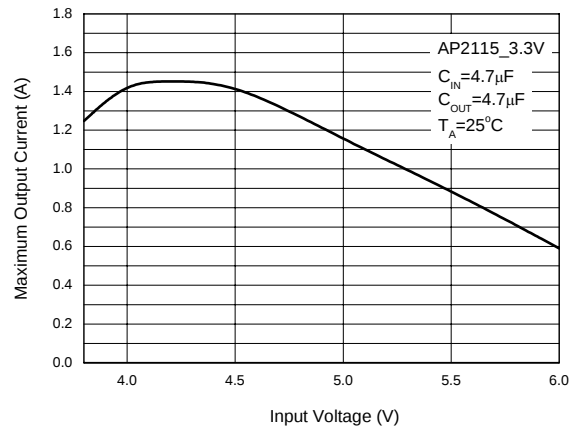


Figure 19. Maximum Output Current vs. Input Voltage

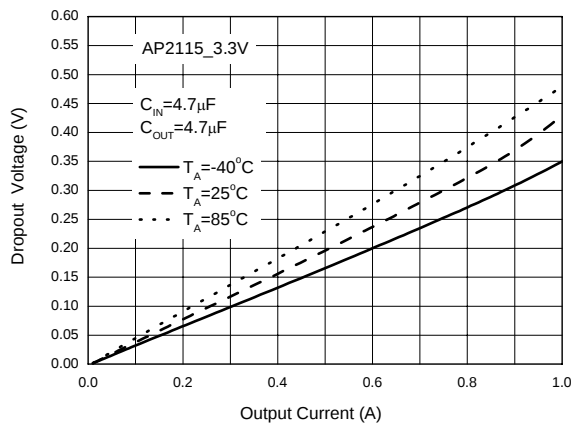
**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Typical Performance Characteristics (Continued)**

Figure 20. Dropout Voltage vs. Output Current

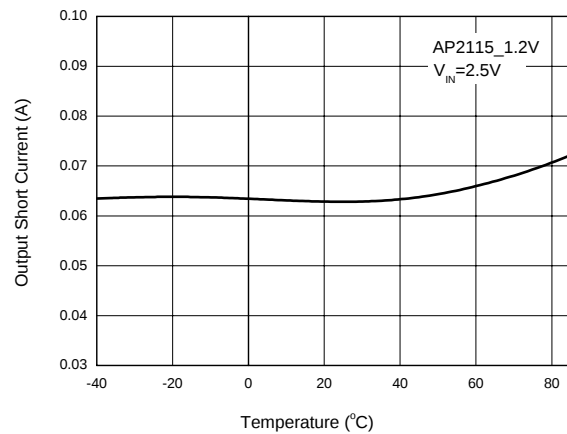


Figure 21. Output Short Current vs. Temperature

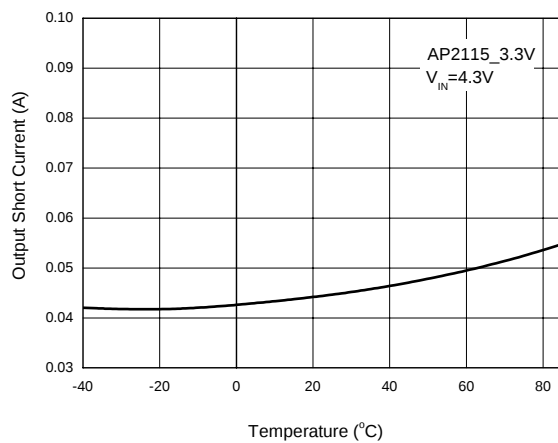


Figure 22. Output Short Current vs. Temperature

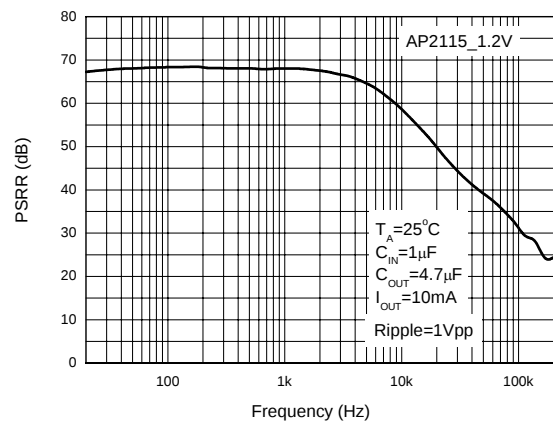


Figure 23. PSRR vs. Frequency

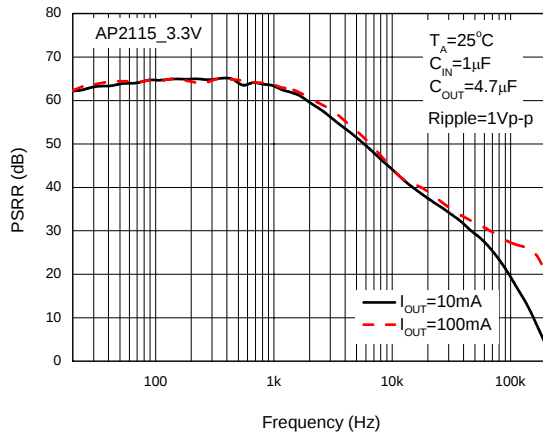
**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Typical Performance Characteristics (Continued)**

Figure 24. PSRR vs. Frequency

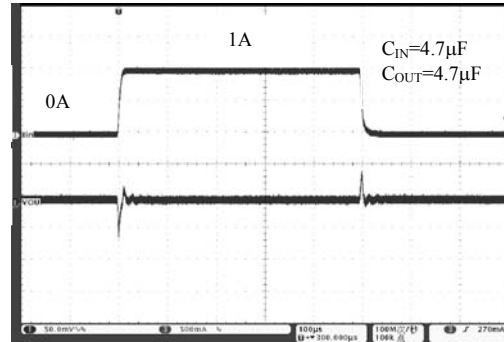
 I_{OUT}
500mA/div V_{OUTAC}
50mV/div

Figure 25. Load Transient

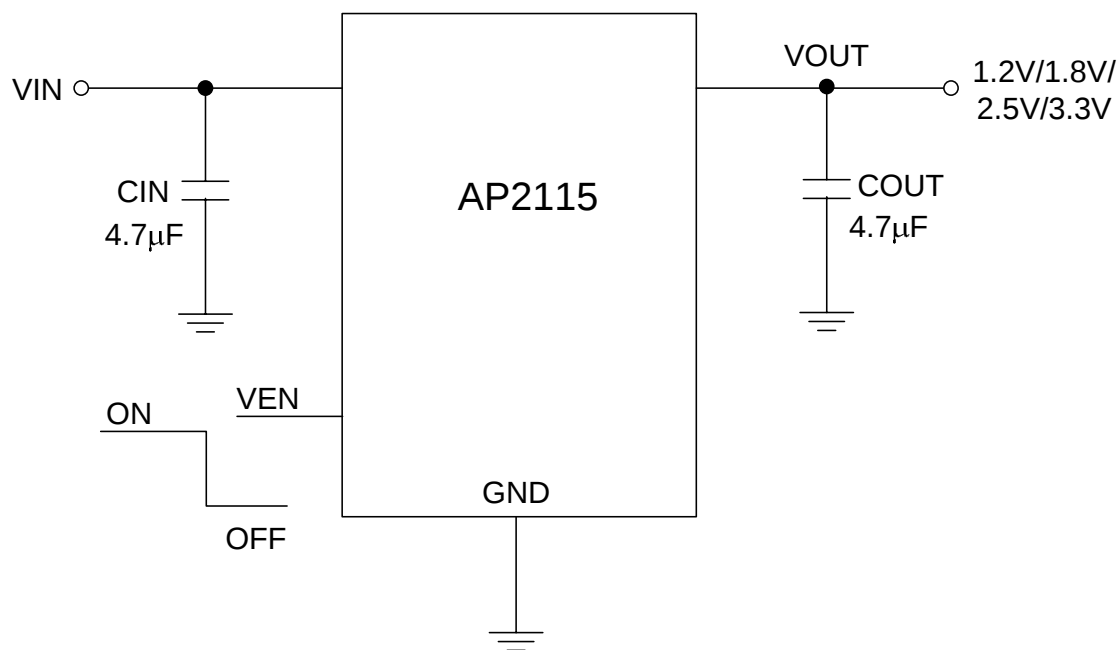
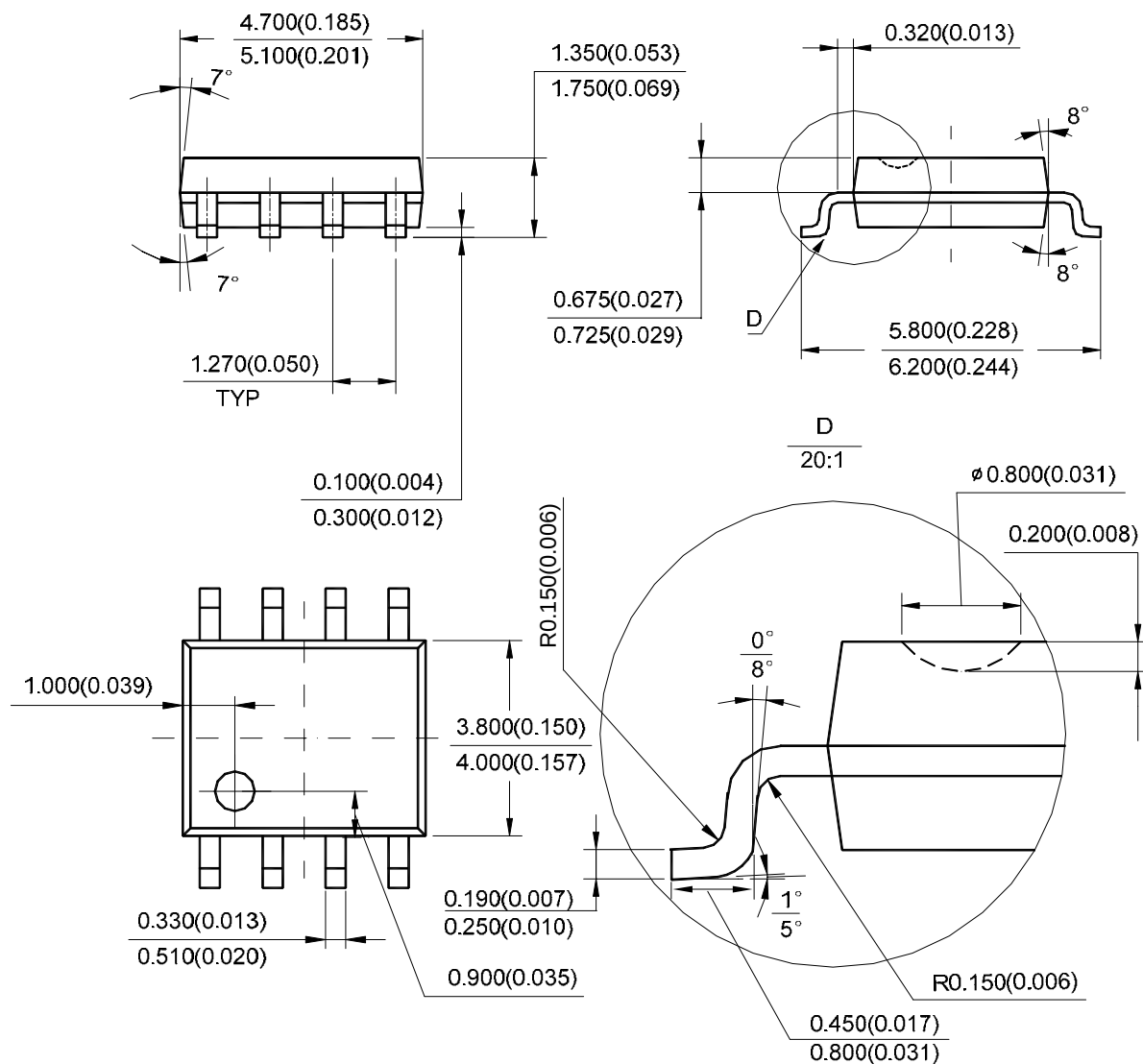
1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115**Typical Application**

Figure 26. AP2115 Typical Application

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115****Mechanical Dimensions****SOIC-8****Unit: mm(inch)**

Note: Eject hole, oriented hole and mold mark is optional.



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2115

Mechanical Dimensions (Continued)

SOT-89-5

Unit: mm(inch)

